Claims

What is claimed is:

1. A semiconductor apparatus for storing a key and data, comprising:

first to N-th (N is a natural number equal to or greater than two) storage sections having first to N-th storage capacities, respectively, the storage sections:

storing an externally-input key or data at a received address in key-and-data writing; and

when a key and data are stored at a received address, outputting the key and data; and

when a key or data is not stored at a received address, outputting a first signal indicating that a key or data is not stored at the received address, in key-and-data reading;

first to N-th comparison sections, the comparison sections:

comparing the externally input key with keys output from the first to N-th storage sections; and

when the externally input key matches the keys output from the first to N-th storage sections, outputting a second signal indicating that the externally input key matches the keys output from the first to N-th storage sections; and

when the first to N-th storage sections output the first signals, outputting a third signal indicating that the first to N-th storage sections output the first signals, in key-and-data writing into the first to N-th storage sections; and

comparing the externally input key with keys output from the first to N-th storage sections; and

when the externally input key matches the keys output from the first to N-th storage sections, externally outputting data output from a storage section which outputs the key that matches the externally input key, among the first to N-th storage sections, in key-and-data reading from the first to N-th storage sections;

a first calculation section performing a first calculation which associates the externally input key with a first address in many-to-one correspondence;

a second calculation section performing a second calculation which associates the first address with a second address in one-to-one correspondence;

a first processing section operating when a key and data are written, the first processing section:

sending the first address to the first to N-th storage sections; and

when the second signal is received from the M-th (M is a natural number equal to or less than N) comparison section, storing the externally input data at the first address in the M-th storage section;

when the second signal is not received from any of the first to N-th comparison sections and the third signal is received from one or more of the first to N-th comparison sections, storing the externally input key and data at the first address in the first storage section obtained when a storage section or storage sections that output the first signal among the first to N-th storage sections are arranged in a first order;

when the second signal is not received from any of the first to N-th comparison sections and the third signal is not received from any of the first to N-th comparison sections, sending the second address to the first to N-th storage sections;

when the second signal is received from the L-th (L is a natural number equal to or less than N) comparison section, storing the externally input data at the second address in the L-th storage section; and

when the second signal is not received from any of the first to N-th comparison sections and the third signal is received from one or more of the first to N-th comparison sections, storing the externally input key and data at the second address in the first storage section obtained when a storage section or storage sections that output the first signal among the first to N-th storage sections are arranged in a second order; and

a second processing section operating when data is read, the second processing section:

sending the first address to the first to N-th storage sections; and

when the second signal is not received from any of the first to N-th comparison sections, sending the second address to the first to N-th storage sections.